

1 CLAIM LISTING

2 1. (Currently Amended) A communications bus connected between a source node and a
3 destination node, the communications bus including:

4 (a) a number of alternate transmission paths extending between the source node and
5 the destination node on a common substrate comprising a semiconductor chip;

6 (b) a source switching arrangement interposed between the source node and the
7 alternate transmission paths, the source switching arrangement being operable to
8 selectively connect the source node to a selected one of the alternate transmission
9 paths and disconnect the source node from each other alternate transmission path;
10 and

11 (c) a destination switching arrangement interposed between the destination node and
12 the alternate transmission paths, the destination switching arrangement being
13 operable to selectively connect the destination node to the selected one of the
14 alternate transmission paths and disconnect the destination node from each other
15 alternate transmission path; and

16 (d) test circuitry connected to the source node and the destination node for applying a
17 test signal to the selected one of the alternate transmission paths and for
18 monitoring the destination node to determine whether the test signal is properly
19 received at the destination node, wherein when the test signal is not properly
20 received at the destination node the source switching arrangement disconnects the
21 source node from the selected one of the alternate transmission paths and connects
22 the source node to a respective one of the other alternate transmission paths, and
23 the destination switching arrangement disconnects the destination node from the

1 selected one of the alternate transmission paths and connects the destination node
2 to the respective one of the other alternate transmission paths.
3

4 2. (Original) The communications bus of Claim 1 wherein:

- 5 (a) the source switching arrangement includes multiple source switching devices, a
6 different source switching device connected between the source node and each
7 alternate transmission path; and
8 (b) the destination switching arrangement includes at least one destination switching
9 device connected between the destination node and each alternate transmission
10 path.
11

12 3. (Currently Amended) The communications bus of Claim [[1]] 2 wherein:

- 13 (a) the different source switching devices include at least one multiplexer; and
14 (b) the at least one destination switching device comprises a multiplexer.
15

16 4. (Original) The communications bus of Claim 1 further including:

- 17 (a) a source switch control structure for controlling the operation of the source
18 switching arrangement; and
19 (b) a destination switch control structure for controlling the operation of the
20 destination switching arrangement.
21

1 5. (Previously Presented) The communications bus of Claim 4 wherein the source switch
2 control structure and the destination switch control structure each includes a nonvolatile
3 or volatile memory structure.

4
5 6. Canceled

6
7 7. (Original) The communications bus of Claim 1 wherein:

8 (a) a receive node and first direction control node are associated with the source node,
9 and a send node and second direction control node are associated with the
10 destination node;

11 (b) a send switching arrangement is interposed between the send node and each
12 alternate transmission path;

13 (c) a receive switching arrangement is interposed between each alternate transmission
14 path and the receive node;

15 (d) a first direction control switching arrangement is interposed between the first
16 direction control node and a control input of a tri-state driver associated with the
17 source node; and

18 (e) a second direction control switching arrangement is interposed between the
19 second direction control node and a control input of a tri-state driver associated
20 with the send node.

1 8. (Original) The communications bus of Claim 1 wherein:

2 (a) the communications bus is also connected between a number of additional source
3 nodes and the same number of additional destination nodes;

4 (b) a number of additional alternate transmission paths extend between each
5 additional source node and each additional destination node;

6 (c) the source switching arrangement is also interposed between each additional
7 source node and the respective alternate transmission paths associated with that
8 respective additional source node, the source switching arrangement also being
9 operable to selectively connect each respective additional source node to a
10 selected one of the additional alternate transmission paths associated with that
11 source node and disconnect each respective additional source node from each
12 other additional alternate transmission path associated with that additional source
13 node; and

14 (c) the destination switching arrangement is also interposed between each additional
15 destination node and the respective alternate transmission paths associated with
16 that additional destination node, the destination switching arrangement also being
17 operable to selectively connect each respective additional destination node to the
18 selected one of the alternate transmission paths associated with that additional
19 destination node and disconnect the respective additional destination node from
20 each other additional alternate transmission path associated with that additional
21 destination node.
22

1 9. (Original) The communications bus of Claim 8 wherein the source switching
2 arrangement comprises a number of multiplexers.

3
4 10. (Original) The communications bus of Claim 9 wherein the source node and number of
5 additional source nodes are arranged side-by-side and wherein at least one pair of
6 adjacent source nodes in this side-by side arrangement share a common multiplexer
7 included in the number of multiplexers.

8
9 11. (Original) The communications bus of Claim 8 wherein:

- 10 (a) the source switching arrangement includes a first switching subset connected to a
11 first subset of the alternate transmission paths;
12 (b) the source switching arrangement further includes a second switching subset
13 connected to a second subset of the alternate transmission paths; and
14 (c) the alternate transmission paths making up the second subset of alternate
15 transmission paths are interleaved with the alternate transmission paths making up
16 the first subset of alternate transmission paths.

17
18 12. (Currently Amended) The communications bus of Claim 8 wherein:

- 19 (a) the source node and each additional source node is associated with a respective
20 receive node and first direction control node, and the destination node and each
21 additional destination node are is associated with a respective send node and
22 second direction control node;

- (b) a send switching arrangement is interposed between the send nodes and the alternate transmission paths;
- (c) a receive switching arrangement is interposed between the alternate transmission paths and the receive nodes;
- (d) a first direction control switching arrangement is interposed between the first direction control nodes and a control input of a number of tri-state drivers, each tri-state driver associated with a respective source node; and
- (e) a second direction control switching arrangement is interposed between the second direction control nodes and a control input of a number of additional tri-state drivers, each additional tri-state driver associated with a respective send node.

13. (Currently Amended) A communications bus connected between a number of source nodes and an equal number of destination nodes where each respective source node is matched with a respective one of the destination nodes to form a respective matched pair of nodes, the communications bus including:

- (a) for each respective matched pair of nodes, a number of alternate transmission paths extending between each the respective source node and [[a]] the respective matched one of the destination nodes included in the respective matched pair of nodes, the number of alternate transmission paths being formed on a common substrate comprising a semiconductor chip, the matched destination node being matched to a respective one of the source nodes;

- 1 (b) a source switching arrangement, the source switching arrangement being
2 interposed between each respective source node and the respective alternate
3 transmission paths associated with that respective source node, the source
4 switching arrangement also being operable to selectively connect each respective
5 source node to a respective selected one of the alternate transmission paths
6 associated with that source node and disconnect each respective source node from
7 each other alternate transmission path associated with that source node; and
8 (c) a destination switching arrangement, the destination switching arrangement being
9 interposed between each respective destination node and the respective alternate
10 transmission paths associated with that respective destination node, the
11 destination switching arrangement also being operable to selectively connect each
12 respective destination node to the respective selected one of the alternate
13 transmission paths associated with that destination node and disconnect the
14 respective destination node from each other alternate transmission path associated
15 with that destination node;
16 (d) wherein each source node is associated with a respective receive node and first
17 direction control node, and each destination node is associated with a respective
18 send node and second direction control node;
19 (e) wherein a send switching arrangement is interposed between the send nodes and
20 the alternate transmission paths;
21 (f) wherein a receive switching arrangement is interposed between the alternate
22 transmission paths and the receive nodes;

- 1 (g) wherein a first direction control switching arrangement is interposed between the
2 first direction control nodes and a respective control input of a number of tri-state
3 drivers, each tri-state driver associated with a respective source node; and
4 (h) wherein a second direction control switching arrangement is interposed between
5 the second direction control nodes and a respective control input of a number of
6 additional tri-state drivers, each additional tri-state driver associated with a
7 respective send node.

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9 14. (Original) The communications bus of Claim 13 wherein the source switching
10 arrangement comprises a number of multiplexers.

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12 15. (Original) The communications bus of Claim 14 wherein the source nodes are arranged
13 side-by-side and wherein at least one pair of adjacent source nodes in this side-by side
14 arrangement share a common multiplexer included in the number of multiplexers.

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16 16. (Original) The communications bus of Claim 13 wherein:

- 17 (a) the source switching arrangement includes a first switching subset connected to a
18 first subset of the alternate transmission paths;
19 (b) the source switching arrangement further includes a second switching subset
20 connected to a second subset of the alternate transmission paths; and
21 (c) the alternate transmission paths making up the second subset of alternate
22 transmission paths are interleaved with the alternate transmission paths making up
23 the first subset of alternate transmission paths.

1 17. Canceled

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3 18. (Currently Amended) A method for compensating for errors in a communications bus
4 between a source node and a destination node, the bus including alternate transmission
5 paths between the source node and destination node on a common substrate, the method
6 including the steps of:

7 (a) applying a test signal to a first one of the alternate transmission paths between the
8 source node and the destination node;

9 (b) determining whether the test signal is properly received at the destination node;
10 and

11 (c) if the test signal is not properly received at the destination node, switching to a
12 second one of the alternate transmission paths between the source node and
13 destination node.
14

15 19. (Original) The method of Claim 18 further including the steps of:

16 (a) applying a second test signal to the second one of the alternate transmission paths
17 between the source node and the destination node; and

18 (b) determining whether the second test signal is properly received at the destination
19 node.
20

21 20. (Original) The method of Claim 18 wherein the communications bus extends between a
22 number of source nodes and a like number of destination nodes, and the bus includes a

1 number of alternate transmission paths between each source node and a respective one of
2 the destination nodes, and wherein the method further includes:

- 3 (a) applying a respective test signal to each alternate transmission path between each
4 respective source node and its respective destination node;
5 (b) determining whether each respective test signal is properly received at the
6 respective destination node; and
7 (c) for each respective test signal that is not properly received at the respective
8 destination node, switching the respective source node to a different one of the
9 alternate transmission paths between the respective source node and destination
10 node.

11
12 21. (Original) The method of Claim 20 wherein the step of switching the respective source
13 node to a different one of the alternate transmission paths between the respective source
14 node and destination node includes applying a control signal to a switching device
15 interposed between the source node and the alternate transmission paths associated with
16 the respective source node.

17
18 22. (Original) The method of Claim 21 wherein each control signal is applied from a
19 memory device associated with the communications bus.

20
21 23. (Previously Presented) A communications bus connected between a source node and a
22 destination node, the communications bus including:

- 1 (a) a number of alternate transmission paths extending between the source node and
2 the destination node on a common substrate comprising a semiconductor chip;
- 3 (b) a source switching arrangement interposed between the source node and the
4 alternate transmission paths, the source switching arrangement being operable to
5 selectively connect the source node to a selected one of the alternate transmission
6 paths and disconnect the source node from each other alternate transmission path;
- 7 (c) a destination switching arrangement interposed between the destination node and
8 the alternate transmission paths, the destination switching arrangement being
9 operable to selectively connect the destination node to the selected one of the
10 alternate transmission paths and disconnect the destination node from each other
11 alternate transmission path;
- 12 (d) test circuitry connected to the source node and destination node for applying a test
13 signal to each alternate transmission path at initialization of the communication
14 bus and for monitoring the destination node to determine whether the respective
15 test signal is properly received at the destination node; and
- 16 (e) wherein a receive node and first direction control node are associated with the
17 source node, and a send node and second direction control node are associated
18 with the destination node;
- 19 (f) a send switching arrangement is interposed between the send node and each
20 alternate transmission path;
- 21 (g) a receive switching arrangement is interposed between each alternate transmission
22 path and the receive node;

1 (h) a first direction control switching arrangement is interposed between the first
2 direction control node and a control input of a tri-state driver associated with the
3 source node; and

4 (i) a second direction control switching arrangement is interposed between the
5 second direction control node and a control input of a tri-state driver associated
6 with the send node.

7
8 24. (Previously Presented) The communication bus of claim 23 wherein the test circuitry is
9 configured to apply the test signal once only.